DEVELOPMENT OF FPGA-BASED TDC WITH WIDE DYNAMIC RANGE FOR MONITORING THE TRIGGER TIMING DISTRIBUTION SYSTEM AT THE KEKB INJECTOR LINAC

MOPB017

T. Suwada, F. Miyahara, K. Furukawa, KEK and SOKENDAI, Tsukuba, Japan

Introduction

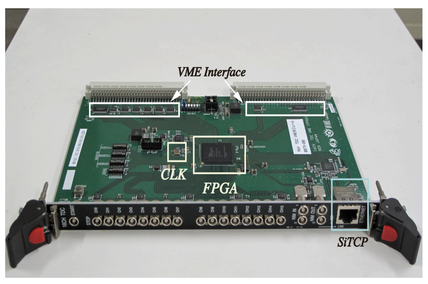
・A new field-programmable gate array (FPGA)-based time-to-digital converter (TDC) with a wide dynamic range greater than 20 ms has been developed to monitor the timing of various pulsed devices in the trigger timing distribution system of the KEKB injector linac.

• For monitoring the timing as precisely as possible, a 16-ch FPGA-based TDC has been developed on a Xilinx Spartan-6 FPGA equipped on VME board with a resolution of 1 ns.

• The resolution was achieved by applying a multisampling technique, and the accuracies were 2.6 ns (rms) and less than 1 ns (rms) within the dynamic ranges of 20 ms and 7.5 ms, respectively.

• The various nonlinear effects were improved by implementing high-precision external clock with a built-in temperature-compensated crystal oscillator.

Basic specifications designed for the FPGA-based TDC



- FPGA:XILINX Spartan-6 (XC6SLX75, DCM 250MHz)
- External clock: EPSON TG-5501CA, 50MHz
- Gigabit ethernet based on SITCP is embedded

Fig.2 : Developed VME/FPGA-based TDC module.

Table 2
Basic specifications designed for the VME/FPGA-based TDC.

Basic parameter	Value	Units
Number of common starts	1	
Number of stops	16	
Number of multistops	4	
Number of bits	32	
Dynamic range (max.)	4.3	s
Resolution	1	ns
Clock frequency	250	MHz
Gigabit ethernet	Available	

Table 3
Specifications of the external clock.

Parameter	Value	Remarks
Clock frequency	50 MHz	
Frequency stability	$< \pm 1.0 \times 10^{-6}$	$T_e = 25 \pm 2$ °C
Temperature characteristics	$< \pm 0.28 \times 10^{-6}$ °C^{-1}	T_e=–40 to 85 °C

Multisampling technique in the time duration measurement

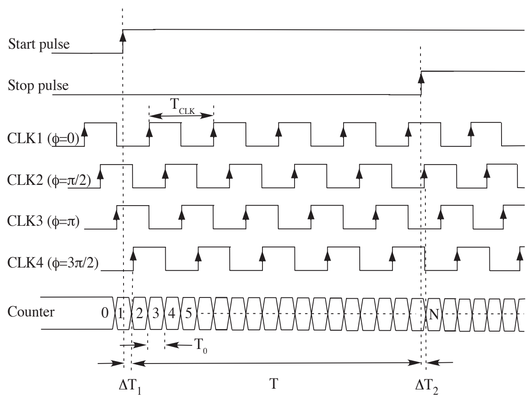


Fig.3 : Timing diagram of the fundamental time-duration measurement of the TDC based on the multisampling technique.

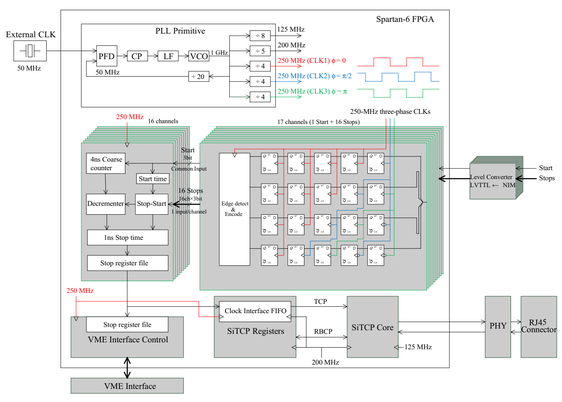


Fig.4 : Schematic block diagram of the circuit architecture of the developed TDC.

Characteristics evaluations of the TDC module

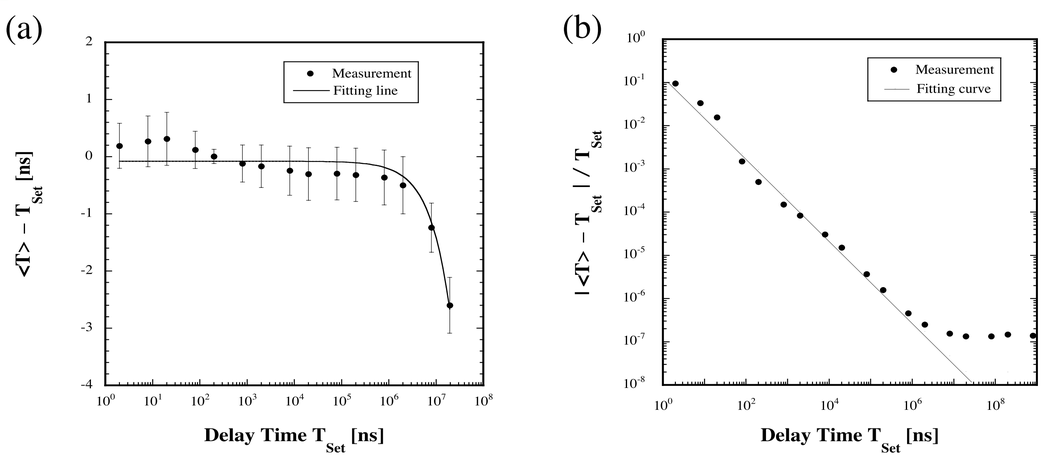


Fig. 5 (a) : Variations in the time difference (nonlinearity) between the measured and set delay time with a dynamic range of 20ms. Each solid point represents the average value over 5000 measurements and only the statistical error bars are plotted. The solid line shows a straight-line fitting in (a).
(b) Variations in the accuracy as a function of the set delay time. The solid line is an exponential function fitted to the data.

Trigger timing distribution system at the KEKB injector linac

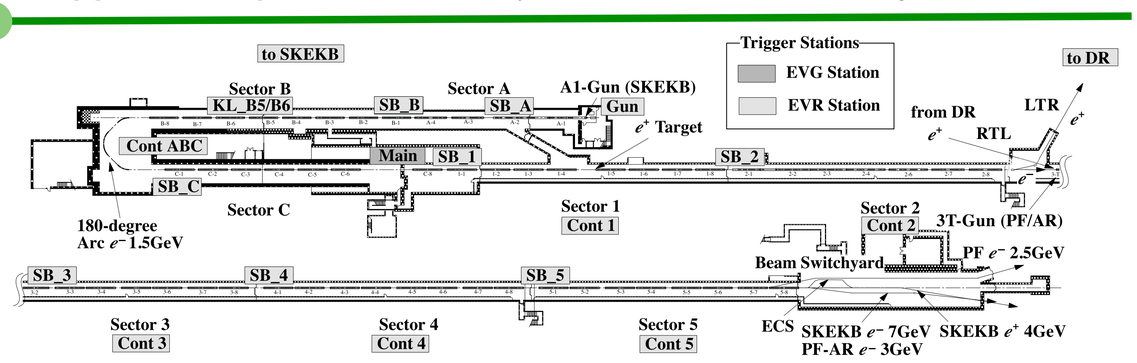


Fig.1 : Schematic layout of the injector linac and the locations of the new trigger timing distribution system.

- The development of the new trigger timing distribution system started in 2004 to realize top-up injections for both the previous KEKB and PF rings based on the new control system.
- This new control system can regulate more than 150 parameters at 50 Hz with an event notification mechanism, and however, it should be further extended in the number of control parameters for the next development including the SuperKEKB, DR, PF, and PF-AR.
- The event notification mechanism is implemented in an event generator-receiver system, which is also called ”event-based timing and control system”.

Table 1
Timing specifications required for the new trigger timing distribution system.

Parameter	Value	Units
Trigger fiducial frequency	50	Hz
RF clock frequency	114.24	MHz
Clock precision (rms)	4.4	ps
Coarse time step	8.75	ns
Fine time step	400	ps
Timing jitter (rms)	10	ps
Delay dynamic range	> 1	s

Characteristics evaluations of the TDC module

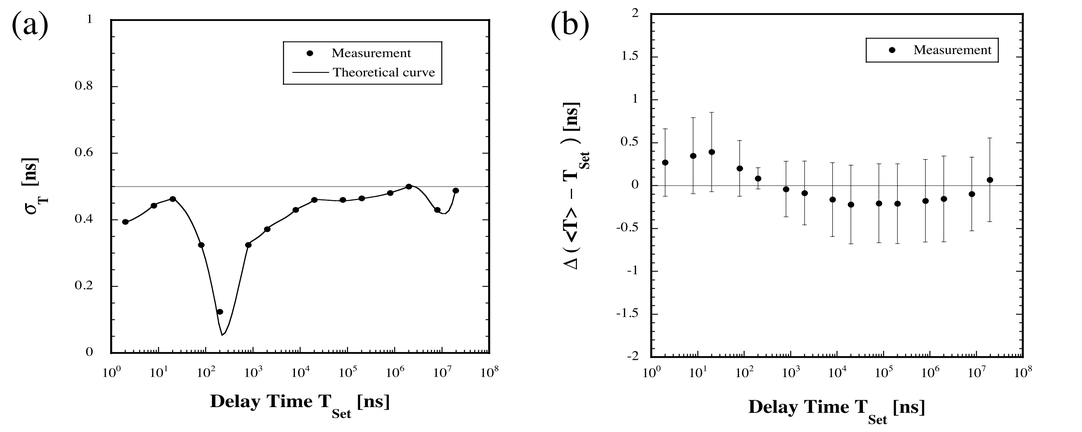


Fig.6 : Variations (a) in the precision measurement depending on the set delay time within a dynamic range of 20 ms and (b) in the differential time difference between the measured and set delay time from a straight-line fitting within the same dynamic range.

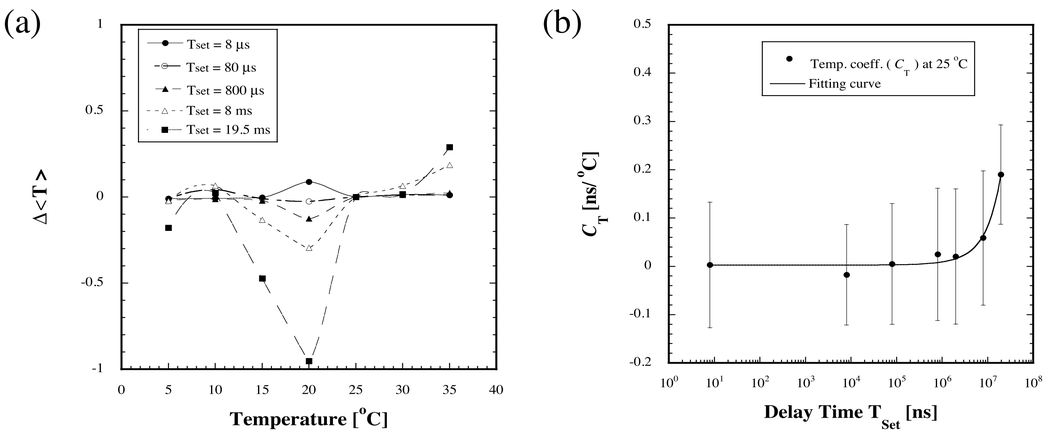


Fig.7 : Variations (a) in the difference between the measured time duration and the set delay as a function of temperature, and (b) in the differential coefficient with temperature as a function of the set delay time. The lines indicate a guide for the eyes only in (a) and a second-order polynomial fit to the experimental data in (b).

Conclusion

- We have successfully fabricated and tested a new VME/FPGA-based TDC with a wide dynamic range greater than 20~ms and a resolution of 1 ns.
- The required specifications of the TDC were realized on the basis of the suitable design with a high-precision temperature-compensated external clock with an accuracy of 0.13 ppm.
- The results are fully sufficient for monitoring the trigger timing distribution system of the injector linac. The developed TDC could be applied to further complex timing systems in large accelerator complexes.