

# Data Acquisition System for SuperKEKB Beam Loss Monitors

MOPB018

Makoto Tobiya, Hitomi Ikeda, John W. Flanagan,

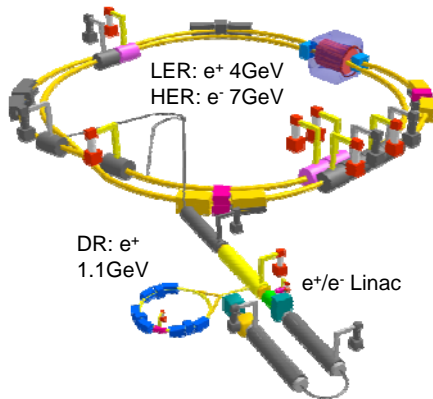
KEK Accelerator Laboratory, 1-1 Oho, Tsukuba 305-0801, Japan

Graduate University for Advanced Studies (SOKENDAI), 1-1, Oho, Tsukuba 305-0801, Japan

## Abstract

The monitoring of the beam loss distribution along the accelerator is important to prevent damage to delicate detectors around the collision point and to vacuum components such as collimators, and also to suppress the unnecessary irradiation of the accelerator elements. As it is not convenient to construct the readout system synchronized to fast timing such as beam injection, a new 64-ch ADC system which samples the output of the loss monitor signal integrator at a fairly fast rate and automatically keep the peak, mean, and minimum data has been developed. The performance of the ADC system is shown. The control system configuration which reads and resets the hardware interlock signal from the loss monitor integrator for the machine protection system (MPS) is also shown.

## SuperKEKB accelerators



Try to achieve x40 larger luminosity from KEKB by

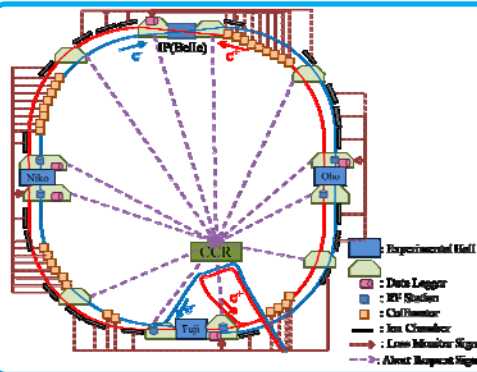
- Double the beam currents
- Reduce beam emittance and x-y couplings
- Squeeze the beam size at IP

## Beam loss

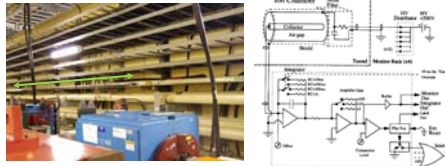
- 50 times larger stable beam loss (10mA/s for LER, 7.2mA/s for HER at maximum lumi.)
- Easy to make fatal damage to both the vacuum components and the BelleII detector due to smaller beam size and higher charge density.

Monitor the beam loss behavior and take necessary actions before causing fatal accidents.

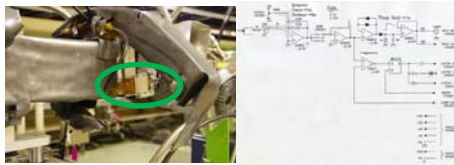
	HER/LER	DR
Energy (GeV)	7/4	1.1
Circumference (m)	3016	135.5
Max. beam current (A)	2.6/3.6	0.08
Number of bunches	2500	4
Single bunch current (mA)	1.04/1.44	18
Bunch separation (ns)	4	>98
Bunch length (mm)	5/6	6
RF frequency (MHz)	508.887	
Harmonic number	5120	230
$\beta^*$ at IP H/V (mm)	25/0.30 32/0.27	-
Horizontal emittance (nm)	4.6/3.2	3.2
X-Y coupling (%)	0.28/0.27	5
Vertical beam size at IP (nm)	59/48	-
Rad. damping time T/L (ms)	58/29 43/22	11/5.4
Max. injection rate (Hz)	50/50	50
Number of Ion Chambers (IC)	105	40
Number of PIN-Photo diodes (PIN)	101	opt.



## Ion Chamber (IC)



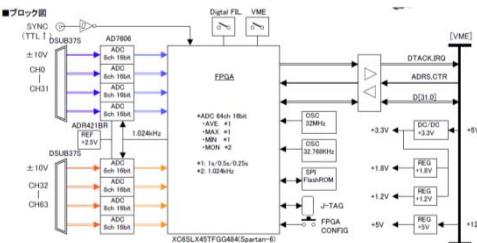
## PIN Photo-diode (PIN)



## Loss monitor readout ADC

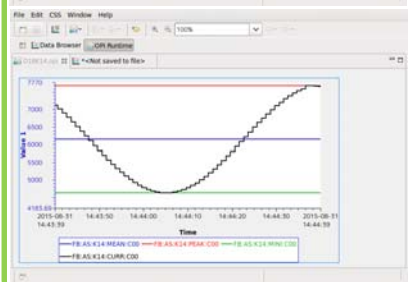
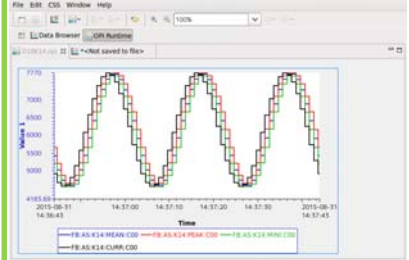
- VME 6U 1W size.
- 64-ch single-ended inputs compatible to old system (+/-10V range, bipolar).
- 16-bit resolution, simultaneous sampling.
- On board peak-hold, minimum-hold, average function with high sampling rate (1kSPS).
- Board to board synchronization function to reset the calculation period.

## Digitex 18K14A 64-ch, 16bit ADC



- 8, 16bit simultaneous sampling ADC (AD7606)
- 1kSPS + up to 64kSPS oversampling
- Spartan6 XC6SLX45 FPGA
- EPICS R314.12.3 device support on VxWorks 6.8.3 + MVME5500

## ADC output (1s scan)



## Synchronization between ADC boards

- Reset the starting time of the calculation (peak, minimum, average) among the distributed 18K14A boards.
- Hardware reset (TTL input on the front panel)
- Software reset (through VME command)
- 45 deg. at peak-to-peak deviation between boards per one day.
- Re-synchronize will be needed 2/day or more.

## Interlock monitor and reset system

- If the beam loss exceeds pre-defined threshold..
- Send beam abort request to MPS.
- Latch the interlock status who triggered the interlock.

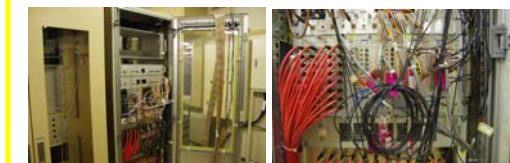
Need to monitor/ to do reset

- Interlock status (TTL)
- Reset the latched interlock to recover the beam.

## Yokogawa FA-M3 I/O control system



32bit TTL Input X 2  
32bit TTL output  
Linux-base CPU with built-in EPICS system



## Summary

We have designed and tested a new 64-ch VME ADC with intrinsic peak, minimum and mean calculation functions for SuperKEKB beam loss monitor systems. Data obtained in the test stand shows excellent performance as expected. The I/O control system to read and reset the interlock status of the loss monitors are also designed and tested and confirmed to be working as expected.

Though the current analog amplifier and integrator unit has long integration or peak-holding functions, the high speed sampling of the developed ADC board might not be so significant. Nevertheless, it might be possible to omit the analog integration circuit which will be installed in the future.