Fast Orbit Feedback FPGA enclosure assembly at the Australian Synchrotron  
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INTRODUCTION

The Fast Orbit Feedback system is being implemented at the Australian Synchrotron as an upgrade to improve electron beam stability, along with the stability of the light source for users. To correct any disturbances within the system while running live, the magnet system at the Australian Synchrotron was to be upgraded with an additional set of coils. The system utilizes information from the Libera Electron BPM electronics at a rate of 10 kHz, the calculations are executed with a Xilinx Vertex 6 FPGA platform and is transmitted to 14 corrector power supplies, one for each sector of the storage ring. The controller unit of the Fast Orbit Feedback was to be installed into a rack mounted enclosure, due to the size of the FPGA unit and associated equipment a 2U 19” enclosure was used in the design of the system. An image of the 3D CAD model is shown in Figure 1.

Figure 1 FOFB FPGA Assembly 3D Model  
Solid Edge software package was used to generate the 3D representation of the equipment being installed, this allowed to measure and design placement of all associated equipment into the 2U 19” enclosure used.

CONSTRUCTION DESIGN LIMITATIONS

- Enclosure type was to be 19” rack mountable for integration into the existing equipment rack
- Enclosure ventilation required to allow air flow and heat dissipation
- Cable entry for signals to be on the back of the unit to allow the equipment rack front door to be closed
- The assembly of the unit was designed to present all possible GPIO to the back panel for external signal connectivity
- Comply to Australian standard IP2X safety

KEY DESIGN FEATURES FOR THE UNIT HARDWARE

- The system is communicating via fibre optic to each of the power supplies
- 14 power supply fibre optic transmitters
- 2 spare transmitting ports
- 2 spare optical receivers
- Communications ports designed to be at the rear of the enclosure to keep the front panel clear for diagnostics. Figure 2 shows the fibre optic communications hardware.

Figure 2 Fibre optic connections for communicating with the power supplies

- Visual representation of diagnostics to be on the front of the enclosure in the form of LEDs and an LCD. Figure 3 below shows the layout of the front panel.

Figure 3 Unit front panel layout

KEY DESIGN FEATURES FOR NEW SYSTEM (cont.)

- The front panel of the unit incorporates a set of switches and LEDs, this to assist with debugging purposes during commissioning, and can be used for setting system configuration or mode of operations.

Figure 4 Switches and LEDs on the front panel

- Programming the FPGA unit can be done via the USB-B connector on the front panel which connects directly to the JTAG unit
- The USB-A connections allow access to the USB connectors mounted on the FPGA processor card. Figure 5 shows the JTAG interface unit installed within the unit.

Figure 5 JTAG interface unit

- The back panel of the unit has GPIO presented for any additional signals or interlocks
- The SMA connections are to be used for high speed timing signals, along with system timing signals. Figure 6 shows the layout of the GPIO on the back panel of the unit.

Figure 6 GPIO layout and General Purpose triggers/synchronisation signals

FUTURE DEVELOPMENTS

The Fast Orbit Feedback system will be installed and commissioned in early 2016, all associated cabling and equipment is installed and ready for testing. Additional units will be assembled for development of new systems, and as a test unit for any future developments with the Fast Orbit Feedback.

An additional FPGA processing unit can be utilized in the future to deliver extra computing power for advancements in signal analysis.